CLAIMS

What is claimed is:

1. A method of noise analysis and correction of noise violations for an integrated circuit design comprising steps of:

(a) receiving as input a standard parasitic exchange file for an integrated circuit design;

(b) parsing the standard parasitic exchange file to generate a resistance graph;

(c) generating a representation of the resistance graph to determine noise critical nets;

(d) generating a list of only noise critical nets from the representation of the resistance graph;

(e) selecting a victim net from the list of only noise critical nets;

(f) calculating a value of total crosstalk noise in the selected victim net from all aggressor nets relative to the selected victim net; and

(g) generating as output the value of total crosstalk noise in the selected victim net for correcting a noise violation.

2. The method of Claim 1 wherein step (c) comprises generating one of a resistance tree and a resistance star tree as the representation of the resistance graph.

3. The method of Claim 1 wherein step (d) comprises filtering the nets in the representation of the resistance graph to exclude nets that are not subject to false switching from crosstalk noise.

4. The method of Claim 1 wherein step (d) comprises filtering the nets in the representation of the resistance graph to include nets that drive logical stages that drive noise critical nets.

5. The method of Claim 1 wherein step (f) comprises calculating a peak noise and a drop noise for the selected net.

6. The method of Claim 5 wherein step (f) comprises comparing the peak noise and the drop noise to a peak noise threshold and a drop noise threshold for the selected victim net to determine whether a noise violation may occur in the selected net.

7. The method of Claim 6 wherein step (g) comprises generating a report of a noise violation if the peak noise threshold or the drop noise threshold is exceeded.

8. The method of Claim 7 wherein step (g) comprises reporting a name of the selected victim net, the peak noise, the drop noise, and names of significant

aggressor nets and their respective contributions to the total noise.

9. The method of Claim 1 wherein step (f) comprises calculating a crosstalk noise VX_m coupled into the selected victim net by an aggressor by the following formulas:

$$VX_m = V_{dd} \frac{\tau_{cm}}{\tau_T} \cdot \left(\frac{\tau_T}{\tau_m} \right)^{\frac{\tau_m}{\tau_m - \tau_T}} \quad if \ \tau_m - \tau_T \neq 0 \text{ and}$$

$$VX_m = V_{dd} \frac{\tau_{cm}}{\tau_T} \cdot e^{-1} \quad if \ \tau_m - \tau_T = 0 \ .$$

10. The method of Claim 9 wherein step (f) comprises calculating a ratio r_m of a coupling capacitance C_{cm} to a total net capacitance C_{vT} so that the crosstalk noise VX_m is given by:

$$VX_m = r_m \cdot V_{dd} \cdot \left(\frac{\tau_T}{\tau_m} \right)^{\frac{\tau_m}{\tau_m - \tau_T}} \quad if \ \tau_m - \tau_T \neq 0 \text{ and}$$

$$VX_m = r_m \cdot V_{dd} \cdot e^{-1} \quad if \ \tau_m - \tau_T = 0 \ .$$

11. The method of Claim 1 further comprising a step of selecting an equivalent transient resistance of

an aggressor net as an aggressor driver resistance for worst case, best case, and nominal case operating conditions from a cell library.

12. The method of Claim 1 further comprising a step of determining values of a peak noise threshold and a drop noise threshold for the selected net and storing the values in a cell library.

13. The method of Claim 1 wherein step (g) further comprises correcting a noise violation in the integrated circuit design by modifying a floorplan of the integrated circuit design wherein modifying the floorplan comprises at least one of increasing driver power of the selected victim net, decreasing driver power of an aggressor net, inserting a buffer in the victim net to reduce net delay, inserting a buffer in at least one of the aggressor nets to reduce net delay, and re-routing the victim net and its aggressors.

14. A computer program product for analyzing noise and correcting noise violations for an integrated circuit design comprising:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) receiving as input a standard parasitic exchange file for an integrated circuit design;

(b) parsing the standard parasitic exchange file to generate a resistance graph;

(c) generating a representation of the resistance graph to determine noise critical nets;

(d) generating a list of only noise critical nets from the representation of the resistance graph;

(e) selecting a net from the list of only noise critical nets;

(f) calculating a value of total crosstalk noise in the selected net from all aggressor nets relative to the selected net; and

(g) generating as output the value of total crosstalk noise in the selected net for correcting a noise violation.

15. The computer program product of Claim 14 wherein step (c) comprises generating one of a resistance tree and a resistance star tree as the representation of the resistance graph.

16. The computer program product of Claim 14 wherein step (d) comprises filtering the nets in the representation of the resistance graph to exclude nets that are not subject to false switching from crosstalk noise.

17. The computer program product of Claim 14 wherein step (d) comprises filtering the nets in the

representation of the resistance graph to include nets that drive logical stages that drive noise critical nets.

18. The computer program product of Claim 14 wherein step (f) comprises calculating a peak noise and a drop noise for the selected net.

19. The computer program product of Claim 18 wherein step (f) comprises comparing the peak noise and the drop noise to a peak noise threshold and a drop noise threshold for the selected net to determine whether a noise violation may occur in the selected net.

20. The computer program product of Claim 19 wherein step (g) comprises generating a report of a noise violation if the peak noise threshold or the drop noise threshold is exceeded.

21. The computer program product of Claim 20 wherein step (g) comprises reporting a name of the selected net, the peak noise, the drop noise, and names of significant aggressor nets and their respective contributions to the total noise.

22. The computer program product of Claim 14 wherein step (f) comprises calculating a crosstalk noise VX_m coupled into the selected net by an aggressor by the following formulas:

$$VX_m = V_{dd} \frac{\tau_{cm}}{\tau_T} \cdot \left(\frac{\tau_T}{\tau_m} \right)^{\frac{\tau_m}{\tau_m - \tau_T}} \quad if \ \tau_m - \tau_T \neq 0 \text{ and}$$

$$VX_m = V_{dd} \frac{\tau_{cm}}{\tau_T} \cdot e^{-1} \quad if \ \tau_m - \tau_T = 0 \ .$$

23. The computer program product of Claim 22 wherein step (f) comprises calculating a ratio r_m of a coupling capacitance C_{cm} to a total net capacitance C_{vT} so that the crosstalk noise VX_m is given by:

$$VX_m = r_m \cdot V_{dd} \cdot \left(\frac{\tau_T}{\tau_m} \right)^{\frac{\tau_m}{\tau_m - \tau_T}} \quad if \ \tau_m - \tau_T \neq 0 \text{ and}$$

$$VX_m = r_m \cdot V_{dd} \cdot e^{-1} \quad if \ \tau_m - \tau_T = 0 \ .$$

24. The computer program product of Claim 14 further comprising a step of selecting an equivalent transient resistance of an aggressor net as an aggressor driver resistance for worst case, best case, and nominal case operating conditions from a cell library.

25. The computer program product of Claim 14 further comprising a step of determining values of a peak noise threshold and a drop noise threshold for the selected net and storing the values in a cell library.

26. The computer program product of Claim 14 wherein step (g) further comprises correcting a noise violation in the integrated circuit design by modifying a floorplan of the integrated circuit design wherein modifying the floorplan comprises at least one of:

increasing driver power of the selected victim net;

decreasing driver power of an aggressor net;

inserting a buffer in the victim net to reduce net delay;

inserting a buffer in at least one of the aggressor nets to reduce net delay; and

re-routing the victim net and its aggressors.

27. A method of noise analysis and correction of noise violations for an integrated circuit design comprising steps of:

(a) receiving as input a standard parasitic exchange file for an integrated circuit design;

(b) parsing the standard parasitic exchange file to generate a resistance graph;

(d) generating a list of only noise critical nets from the representation of the resistance graph;

(c) calculating a value of total crosstalk noise in a selected victim net in the list of noise critical nets from all aggressor nets relative to the selected victim net; and

(d) generating as output the value of total crosstalk noise in the selected victim net for correcting a noise violation.